



ATTORNEY'S DOCKET NO.: S1022.80938US01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Philippe JOUEN and Michael KRAEMER
Serial No.: 10/675,810
Filed: September 30, 2003
For: PHASE-LOCKED LOOP WITH HIGH FREQUENCY ADJUSTMENT OF THE
OPERATING RANGE OF THE OSCILLATOR

Examiner: David C. Mis
Art Unit: 2817

Confirmation No.: 2225

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR PRIORITY ACKNOWLEDGEMENT
AND REQUEST TO CORRECT TITLE

Sir:

Applicants respectfully request that the Patent and Trademark Office acknowledge receipt of the certified copy of French application No. 0111472 to which this application claims priority. Priority under 35 U.S.C. §119 was claimed when this continuation application was filed on September 30, 2003.

The certified copy of French application No. 0111472 was filed on September 18, 2002 in the parent case, Serial No. 10/235,902, now abandoned.

In support of this request, Applicants enclose highlighted copies of the transmittal letter which accompanied the original submission of the certified copy of French application No. 0111472, the first three pages of the certified copy which bear the application No. 0111472 and the return receipt postcard indicating its receipt at the Patent Office. Also enclosed is a copy of page 1 of the present application-as-filed identifying the present application as a continuation of Serial No. 10/235,902.

Prompt acknowledgment of the submission of the priority document is respectfully requested.

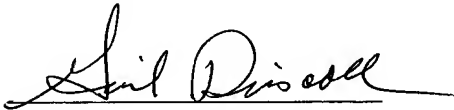
Page 2, paragraph 1, of the Office Action mailed from the Patent Office on September 28, 2004 states, "The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed". A copy of page 2 of the September

28, 2004 Office Action is enclosed. In the response to this Office Action, mailed December 23, 2004, Applicants amended the title to read: "Phase-Locked Loop With High Frequency Adjustment Of The Operating Range Of The Oscillator". A copy of page 2 of the December 23, 2004 amendment is also enclosed. Accordingly, Applicants request that the title be changed prior to the printing of the issued patent to incorporate the new title as required by the Examiner.

Should any questions arise concerning the foregoing, please contact the undersigned at the telephone number listed below.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the 28th day of April, 2005.



Attorney Docket No.: S1022.80938US01

Respectfully submitted,

Philippe Jouen et al., Applicant

By: 

James H. Morris

Reg. No.: 34,681

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S1022.80938US01

-1-

Express Mail Label No. EV 292561971 US
Mailed : September 30, 2003**COPY
AS FILED****PHASE-LOCKED LOOP MADE IN INTEGRATED CIRCUIT FORM****Background Of The Invention****RELATED APPLICATIONS**

This application is a continuation of U.S. Application serial no. 10/235,902
5 entitled Phase-Locked Loop Made In Integrated Circuit Form filed on September 5,
2002, which is herein incorporated by reference in its entirety.

1. Field of the Invention

The present invention relates to phase-locked loops, and in particular to a phase-
10 locked loop made in an integrated circuit.

2. Discussion of the Related Art

Fig. 1 schematically shows a phase-locked loop conventionally used in frequency
synthesis. The phase-locked loop includes a voltage-controlled oscillator (VCO) 2
15 generating a periodic output signal of frequency F_{out} to be synchronized on a reference
frequency F_{ref} . A comparison circuit 4 compares a signal with reference frequency F_{ref}
and with a frequency signal F_{div} equal to a division of frequency F_{out} by a
predetermined factor N . Comparison circuit 4 provides a control signal to an integrator
low-pass filter 6. Filter 6 provides a voltage V_{com} for controlling oscillator 2.
20 Frequency F_{out} varies between minimum and maximum frequencies, in an operating
range characteristic of the oscillator, when voltage V_{com} varies between minimum and
maximum values.

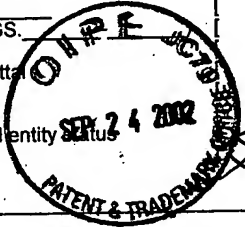
The phase-locked loop is made in an integrated circuit, except for filter 6, as will
be seen hereafter. The characteristics of the integrated components may vary along with
25 the manufacturing process. In particular, the operating range of oscillator 2 may vary
along with the manufacturing process, which may cause a malfunction of the phase-
locked loop. To solve this problem, the operating range of oscillator 2 is adjustable by an
adjustment signal FA , generated by a control and adjustment circuit 8. Circuit 8 is
provided to control whether the oscillator is in a desired operating range or not. For this
30 purpose, circuit 8 ensures that voltage V_{com} of oscillator 2 does not have a value greater



Serial No. 101035902 File No. 501022180938 By: JHM
Title: Phase-Locked Loop MADE IN INTEGRATED CIRCUIT FORM
Application of Philippe Javen et al. WGS Date: NDD

The U.S. PTO Mail Room acknowledges receipt of the following on the date stamped hereon:

<input type="checkbox"/> Mailing by Express Mail (37 CFR 1.10)	<input type="checkbox"/> Provisional Application Cover Sheet
<input type="checkbox"/> Express Mail Label No. _____	<input type="checkbox"/> Multiple Dependent Claim Fee Sheet
<input type="checkbox"/> Patent Application	<input type="checkbox"/> Inf. Disc. Statement, PTO Form 1449
<input type="checkbox"/> Non-provisional <input type="checkbox"/> Provisional	<input type="checkbox"/> References Cited
Incl. _____ pages, (_____ pgs) Specification,	<input checked="" type="checkbox"/> Priority Document(s) # <u>01/11472</u>
(_____ pgs) Abstract, (_____ pgs) Claims (_____ # claims)	<input type="checkbox"/> Copy of Notice to File Missing Parts
<input type="checkbox"/> Design Patent Application	<input type="checkbox"/> Amendment/Response
<input checked="" type="checkbox"/> Declaration(s) <u>01/18</u>	<input type="checkbox"/> Petition for Ext. of Time (x2)
<input checked="" type="checkbox"/> Drawings _____ Sheet(s) (FIGS. _____)	<input type="checkbox"/> Issue Fee Transmittal
<input type="checkbox"/> Formal <input type="checkbox"/> Informal	<input type="checkbox"/> Letter to Official Draftsperson
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<input type="checkbox"/> Fee calculation sheet (x2)	<input type="checkbox"/> Brief (x3)
<input type="checkbox"/> CPA Transmittal	<input type="checkbox"/> Check for \$ _____ Check # _____
<input type="checkbox"/> Verified Statement claiming small entity status	<input type="checkbox"/> Transmittal Letter (x2)
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<input type="checkbox"/> Other _____	



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ATTORNEY'S DOCKET NO.: S01022/80938

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Philippe JOUEN and Michael KRAEMER
Serial No.: 10/235,902
Filed: September 5, 2002
For: PHASE-LOCKED LOOP MADE IN INTEGRATED CIRCUIT FORM

Examiner: Unassigned
Art Unit: Unassigned

Confirmation No. Unassigned

Commissioner for Patents
Washington, D.C. 20231

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

- ☒ Declaration and Power of Attorney
- ☒ Certified Copy of French Priority Application No. 01 11472
- ☒ Return Post Card

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617)720-3500, Boston, Massachusetts.

No check is enclosed. If it is determined that a fee is necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to the Commissioner for Patents, Washington, D.C. 20231 on September 18, 2002.

Attorney Docket No.: S01022/80938
XNDD

Respectfully submitted,

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600 Atlantic Avenue
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BREVET D'INVENTION

CERTIFICAT D'UTILITÉ - CERTIFICAT D'ADDITION

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Le Directeur général de l'Institut national de la propriété industrielle certifie que le document ci-annexé est la copie certifiée conforme d'une demande de titre de propriété industrielle déposée à l'Institut.

Fait à Paris, le 29 AOUT 2002

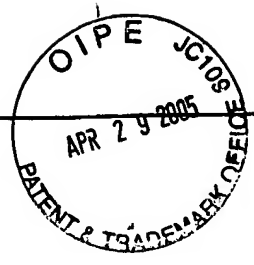
Pour le Directeur général de l'Institut
national de la propriété industrielle
Le Chef du Département des brevets

Martine PLANCHE

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s, rue de Saint Pétersbourg
0 Paris Cedex 08
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REQUÊTE EN DÉLIVRANCE 1/2

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Cet imprimé est à remplir lisiblement à l'encre noire

REMISE DES PIÈCES
DATE **5 SEPT 2001**
LEU **38 INPI GRENOBLE**
N° D'ENREGISTREMENT
NATIONAL ATTRIBUÉ PAR L'INPI **0111472**
DATE DE DÉPÔT ATTRIBUÉE **05 SEP. 2001**
PAR L'INPI
Vos références pour ce dossier
(facultatif) **B5185**

1 NOM ET ADRESSE DU DEMANDEUR OU DU MANDATAIRE À QUI LA CORRESPONDANCE DOIT ÊTRE ADRESSÉE

Cabinet Michel de Beaumont
1 rue Champollion
38000 GRENOBLE

Confirmation d'un dépôt par télécopie ☐ N° attribué par l'INPI à la télécopie

2 NATURE DE LA DEMANDE
Cochez l'une des 4 cases suivantes
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Demande de brevet initiale N° / /
ou demande de certificat d'utilité initiale N° / /
Transformation d'une demande de brevet européen ☐
Demande de brevet initiale N° / /

3 TITRE DE L'INVENTION (200 caractères ou espaces maximum)

BOUCLE À VERROUILLAGE DE PHASE RÉALISÉE SOUS FORME DE CIRCUIT INTÉGRÉ

4 DÉCLARATION DE PRIORITÉ OU REQUÊTE DU BÉNÉFICE DE LA DATE DE DÉPÔT D'UNE DEMANDE ANTÉRIEURE FRANÇAISE
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5 DEMANDEUR
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Nom ou dénomination sociale **STMicroelectronics SA**
Prénoms
Forme juridique **Société anonyme**
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Code APE-NAF
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Rue **29, Boulevard Romain Rolland**
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Pays **FRANCE**
Nationalité **Française**
N° de téléphone (facultatif)
N° de télécopie (facultatif)
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BOUCLE À VERROUILLAGE DE PHASE RÉALISÉE SOUS FORME DE CIRCUIT INTÉGRÉ

La présente invention concerne le domaine des boucles à verrouillage de phase, et en particulier une boucle à verrouillage de phase réalisée sous forme de circuit intégré.

La figure 1 représente schématiquement une boucle à verrouillage de phase utilisée de manière classique en synthèse de fréquence. La boucle à verrouillage de phase comprend un oscillateur commandé en tension (VCO) 2 produisant un signal de sortie périodique de fréquence F_{out} devant être synchronisé sur une fréquence de référence F_{ref} . Un circuit de comparaison 4 compare un signal à la fréquence de référence F_{ref} et un signal de fréquence F_{div} égale à une division de la fréquence F_{out} par un facteur N prédéterminé. Le circuit de comparaison 4 fournit un signal de commande à un filtre intégrateur et passe bas 6. Le filtre 6 fournit un potentiel V_{com} de commande de l'oscillateur 2. La fréquence F_{out} varie entre des fréquences minimale et maximale, dans une plage de fonctionnement caractéristique de l'oscillateur, lorsque le potentiel V_{com} évolue entre des valeurs minimale et maximale.

La boucle à verrouillage de phase est réalisée sous forme de circuit intégré, à l'exception du filtre 6 comme on le verra par la suite. Les caractéristiques des composants intégrés

Art Unit: 2817

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

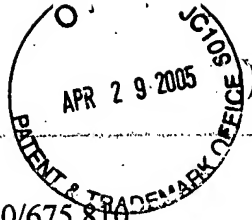
A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 27-31, 35 and 36 are rejected under 35 U.S.C. 102(a.) as being clearly anticipated by Matsuno.

Matsuno disclosed a method of operating a PLL (title) comprising a VCO (24) controlled by a control signal (control voltage 1), comprising monitoring a value of the control signal (26) and inhibiting the PLL (figures 3, 9) if the monitored value of the control signal is outside a predetermined range of values (figures 2, 7, 8, MONITOR OUTPUT i); first and second reference values for inhibiting the PLL (column 4, line 58 – column 5, line 8; figures 2,



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Serial No.: 10/675,810
Conf. No.: 2817

- 2 -

Art Unit: 2225

IN THE SPECIFICATION

Please amend the title as shown below.

PHASE-LOCKED LOOP WITH HIGH FREQUENCY ADJUSTMENT OF THE OPERATING
RANGE OF THE OSCILLATOR MADE IN INTEGRATED CIRCUIT FORM